International Iberian Nanotechnology Laboratory

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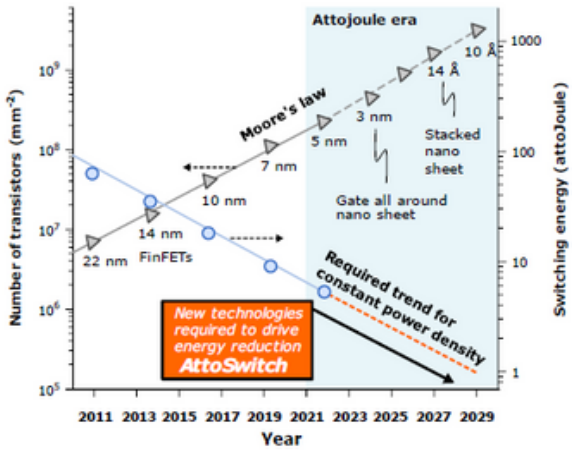
Paulo Ferreira, project responsible at INL

AttoSwitch - developing innovative nanoscale transistors with extremely low energy consumption

INL is part of a new project that will target strategies to impact the semiconductor supply chain at the technology and materials levels to provide ultra-energy-efficient transistors for logic and high-frequency analog integrated chip markets.

Global energy demand for information and communication technologies may reach up to 20% of total energy by the end of the decade. Innovations on transistor technologies, following Moore's law, can in part compensate for this rise and improve sustainability by providing more energy-efficient electronics. However, the energy-efficiency of CMOS is limited by the Boltzmann physics, which sets a lower bound on the operating voltage, and thereby on energy consumption. To sustain miniaturization, and improved performance of electronics, new transistor technologies are needed that can overcome this limit.



AttoSwitch will develop a novel transistor technology, the Dirac FET (DFET) that uses the intrinsically cold carrier distribution of Dirac semimetals (innovative materials with linear dispersion relationship) to overcome the above-mentioned Boltzmann limit. The main objective is to develop a scalable Dirac transistor technology based on large area integration of 2D and 3D Dirac materials (e.g. graphene and CoSi) and the realization of high-performance device demonstrators at technologically relevant length scales.

Press Contact

communication@inl.int

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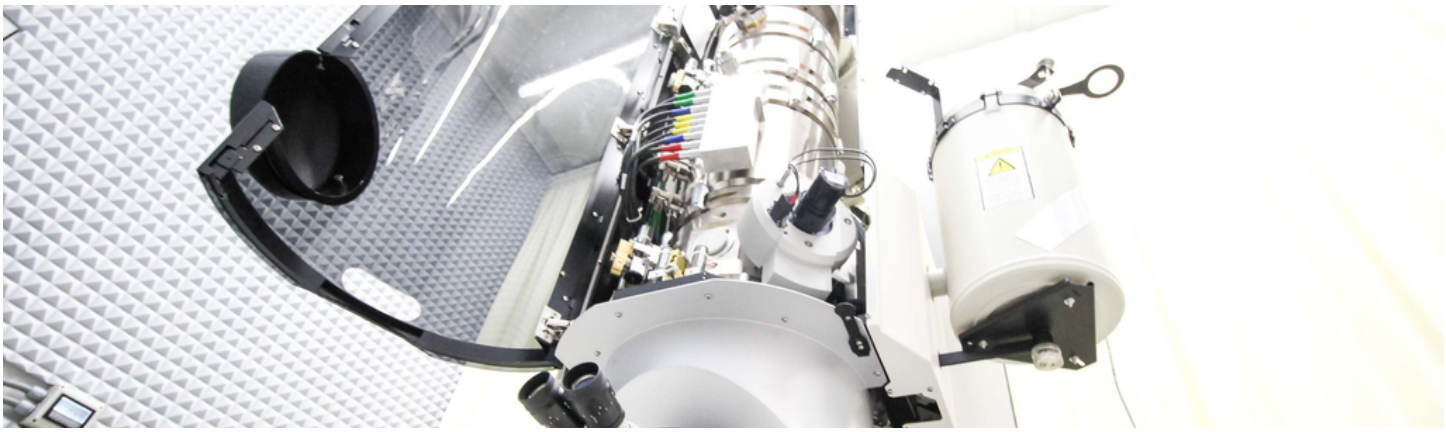
Spotlight on INL science



AttoSwitch consortium comprises six participants ranging from academia to lead semiconductor industries and research centres. The project links to ongoing European efforts, such as the 2D-experimental pilot line, and the goals set by the European Chips Act.

The ambitious performance targets include a subthreshold swing of 35 mV/decade and a switching energy of 4 attojoule. Key demonstrators will be based on graphene integrated with MoS2 and WSe2 channels, as well as novel devices featuring 3D Dirac semimetals.

The project methodology will include development of device process modules and extensive material and device characterization. Systematic modeling using new simulation frameworks will play a key part to benchmark and provide a road map for the technology.

The team at INL is responsible for the advanced characterization of 2D materials and devices. In particular, aberration corrected electron microscopy will be used to understand the atomic structure of 2D and 3D Dirac materials, such as graphene and CoSi, respectively. Paulo Ferreira, the responsible at INL for this project mentions that "This is a very innovative project, involving some of the most prominent groups in the field, where novel transistor technology will be developed to provide electronics with vastly improved energy efficiency at room temperature. As the transistor roadmap will reach the 1 nm node by the end of the decade, it is critical to develop transistors capable of switching with an energy of only one attojoule"

Outreach to students, training of young researchers and building international cooperation will also support Europe's competitiveness in semiconductors.

The 42 months project, that started on January 1st, 2024, has received funding from European Commission-EU under grant agreement n.101135571 and from the Swiss State Secretariat for Education, Research and Innovation (SERI) under contract number no. 23.00594.

The project is coordinated by the "Italian University Nanoelectronics Team" (IUNET consortium) with the Universities of Bologna, Modena/Reggio-Emilia and Udine as affiliated entities.

Project partners are AMO GmbH (Germany), IBM Research GmbH (Switzerland), International Iberian Nanotechnology Laboratory (Portugal), the Interuniversitair micro-electronica centrum vzw (Belgium) and University of Lund (Sweden).
The kick-off meeting has been held in Modena (Italy) on February 21 and 22, 2024.

more about the project
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